a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

62. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to boron penetration at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

67. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si_3N_4) top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

73. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer of approximately a third of the first thickness, which exhibits a high resistance oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

78. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness, wherein the second thickness is [of] less than 12 nanometers (nm).

82. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si_3N_4) top layer of approximately a third of the first thickness, which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness, wherein the second thickness is [of] less than 12 nanometers (nm).

86. (Amended) A logic device and a memory device structure on a single substrate formed by the method comprising:

forming a pair of transistor channel regions on the single substrate;

forming a pair of gate oxides to a first thickness on the pair of channel regions;

wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius;